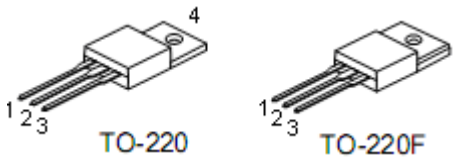
1. Features

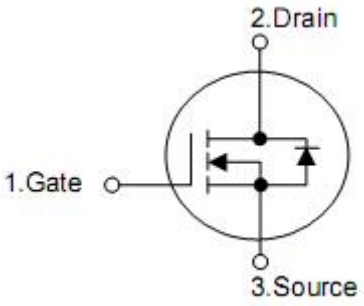
- RoHS Compliant
- $R_{DS(ON)}$,typ.=0.75Ω @ V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

2. Applications

- Adaptor
- Charger
- SMPS Standby Power

3. Pin configuration





Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Ordering Information

Part Number	Package	Brand
KNP6165B	TO-220	KIA
KNF6165B	TO-220F	KIA

5. Absolute maximum ratings

TC=25℃ unless otherwise specified

Parameter	Symbol	TO-220	TO-220F	Unit
Drain-to-Source Voltage	VDSS	650		V
Gate-to-Source Voltage	VGSS	±30		V
Continuous Drain Current	ID	10		A
Pulsed Drain Current at VGS=10V	IDM	40		A
Single Pulse Avalanche Energy	EAS	800		mJ
Power Dissipation	PD	125	45	W
Derating Factor above 25℃		1	0.36	W/℃
Soldering Temperature Distance of 1.6mm from case for 10 seconds	TL	300		℃
Operating and Storage Temperature Range	TJ& TSTG	-55 to 150		℃

6. Thermal characteristics

Parameter	Symbol	TO-220	TO-220F	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.0	2.78	℃/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	100	℃/W

7. Electrical characteristics

(TJ=25°C,unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFF Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	650	--	--	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1	uA
		V_{DS}=520V,V_{GS}=0V,T_J=125℃	--	--	100	uA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=+30V, V_{DS}=0V	--	--	100	nA
		V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
ON Characteristics						
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.0A	--	0.75	0.9	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250uA	2	--	4	V
Forward Transconductance	gfs	V_{DS}=15V,I_D=5.0A	--	8.0	--	S
Dynamic Characteristics(Essentially independent of operating temperature)						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz	--	1650	--	pF
Output Capacitance	C_{oss}		--	125	--	pF
Reverse Transfer Capacitance	C_{rss}		--	13	--	pF
Total Gate Charge	Q_g	V_{DD}=520V, I_D=10A, V_{GS}=0 to 10V	--	30	--	nC
Gate-to-Source Charge	Q_{gs}		--	8	--	nC
Gate-to-Drain (Miller) Charge	Q_{gd}		--	8.5	--	nC
Resistive Switching Characteristics(Essentially independent of operating temperature)						
Turn-on Delay Time	$td_{(ON)}$	V_{DD}=325V, I_D=10A, V_{GS}=10V Rg=4.7Ω	--	10	--	nS
Rise Time	t_{rise}		--	15	--	nS
Turn-Off Delay Time	$td_{(OFF)}$		--	41	--	nS
Fall Time	tf_{all}		--	16	--	nS
Source-Drain Body Diode Characteristics						
Continuous Source Current[2]	I_{SD}	Integral pn-diode in MOSFET	--	--	10	A
Pulsed Source Current[2]	I_{SM}		--	--	40	A
Diode Forward Voltage	V_{SD}	I_S=10A, V_{GS}=0V	--	--	1.5	V
Reverse Recovery Time	trr	V_{GS}=0V I_F=I_S, di/dt=100A/μs	--	455	--	ns
Reverse Recovery Charge	Qrr		--	1.5	--	nC

Note：1.TJ=+25℃ to +150℃
2.Pulse width≤380μs; duty cycle≤2%.

8. Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

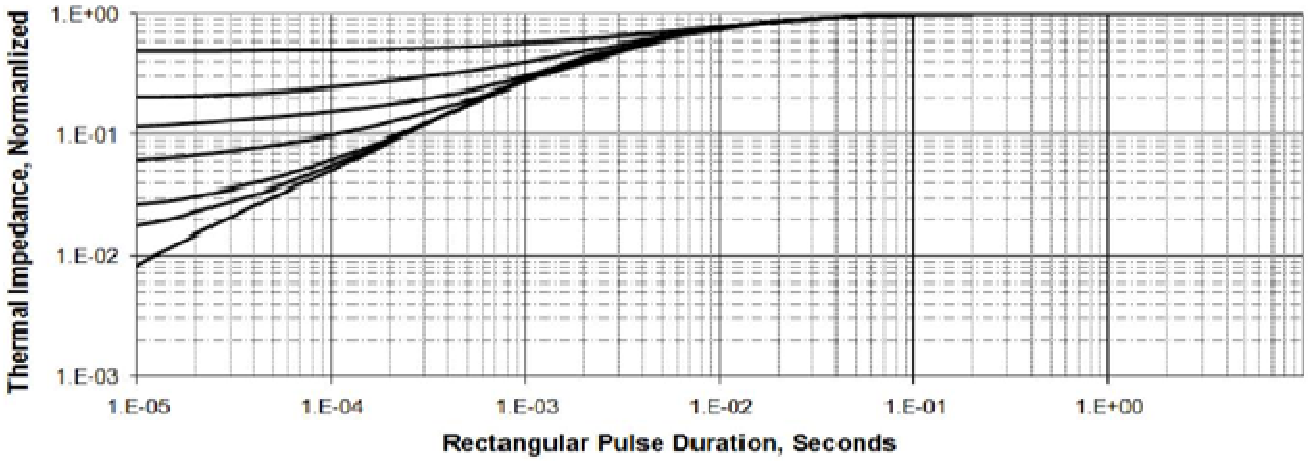


Figure 2 . Max. Power Dissipation vs Case Temperature

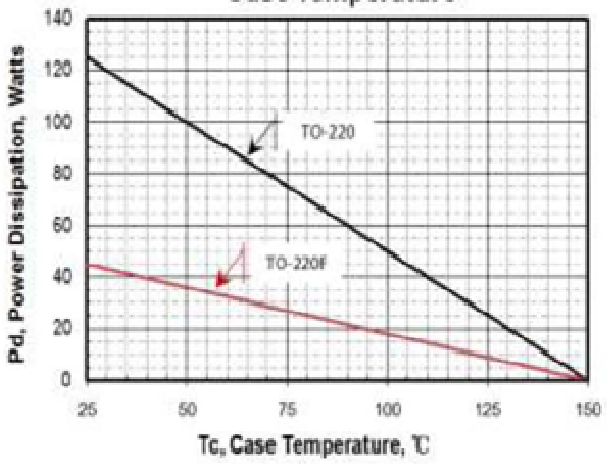


Figure 3 .Maximum Continuous Drain Current vs Tc

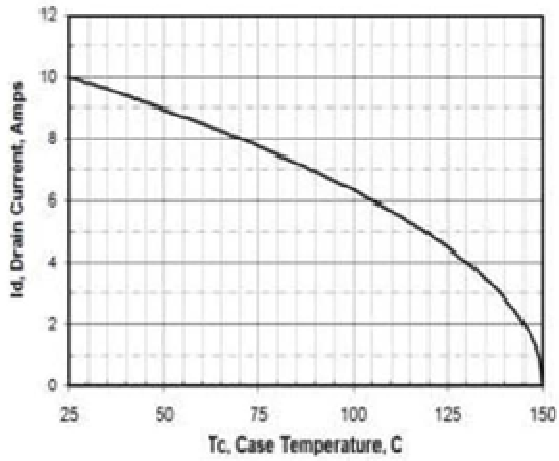


Figure 4. Output Characteristics

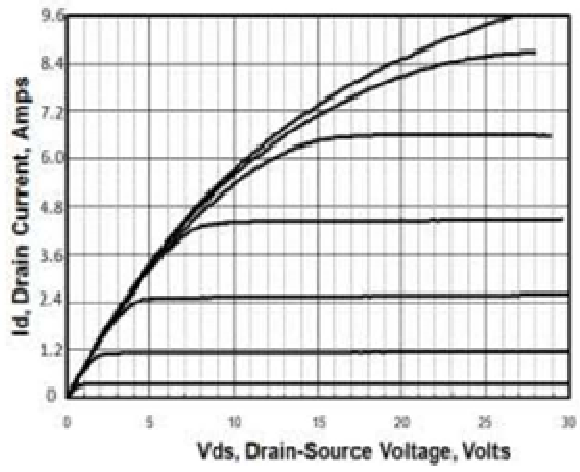


Figure 5. Rdson vs Gate Voltage

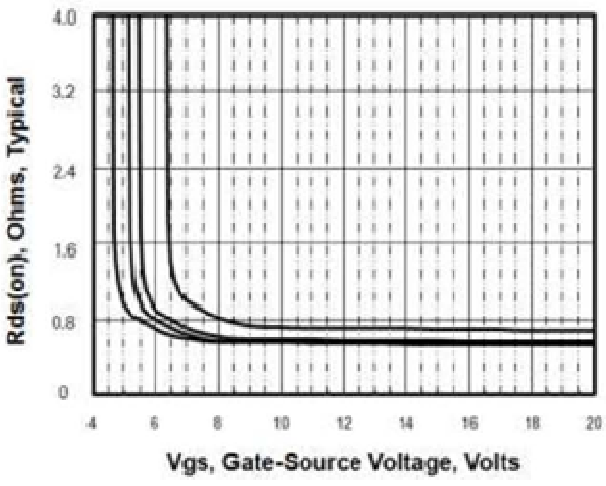


Figure 6. Peak Current Capability

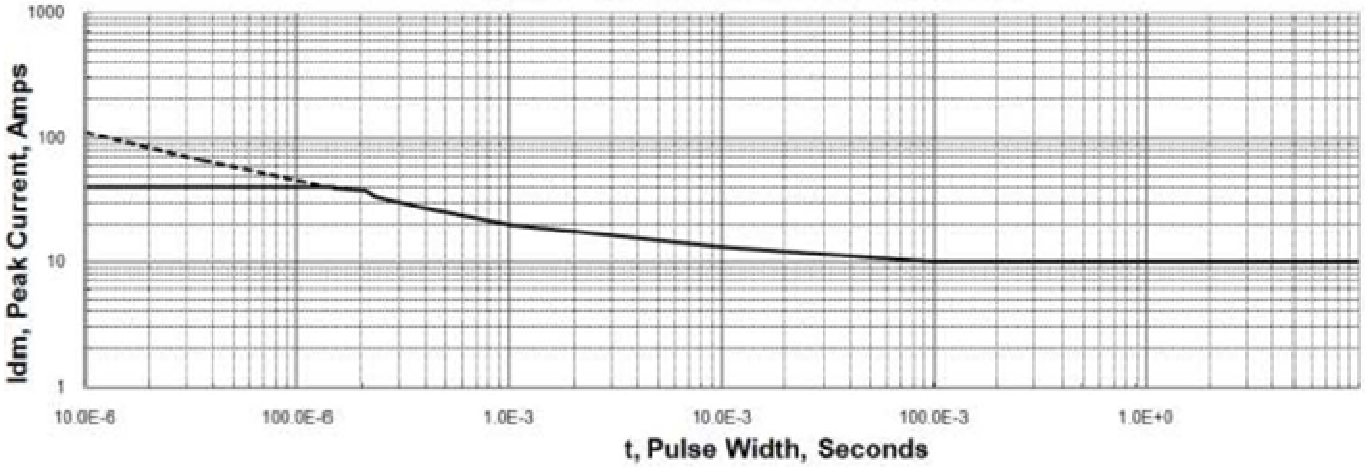


Figure 7. Transfer Characteristics

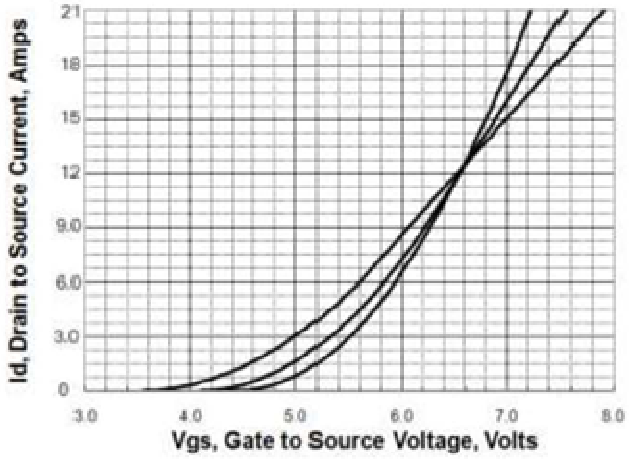


Figure 8. Unclamped Inductive Switching Capability

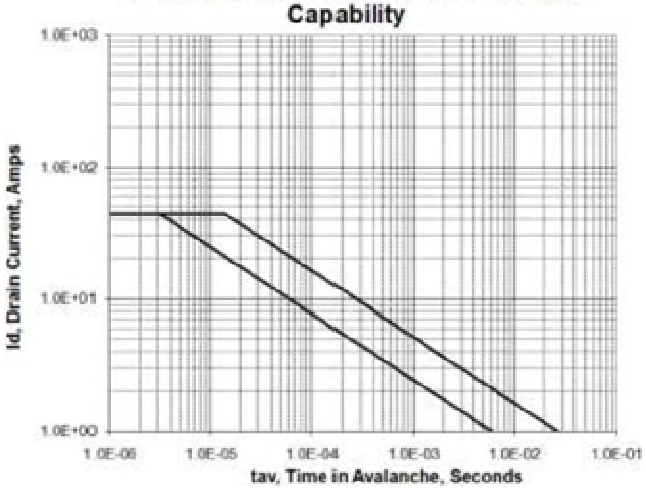


Figure 9. Drain to Source ON Resistance vs Drain Current

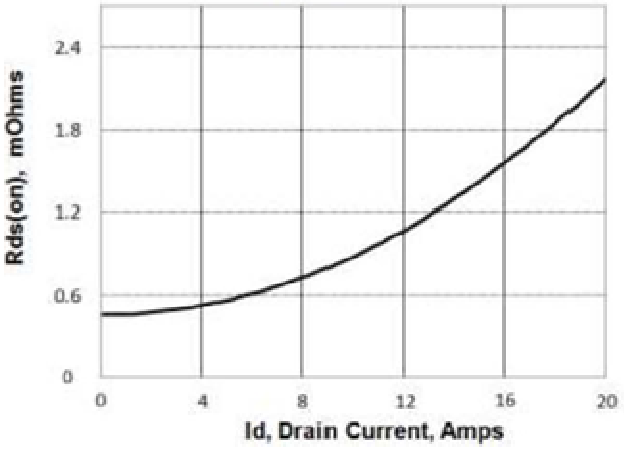


Figure 10. Rdson vs Junction Temperature

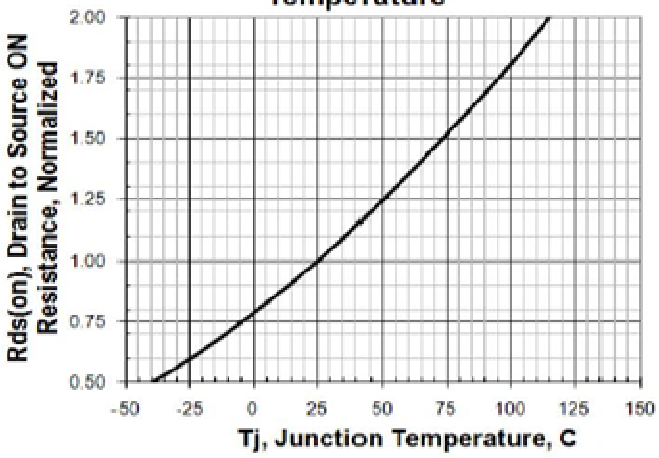


Figure 11.Breakdown Voltage vs Temperature

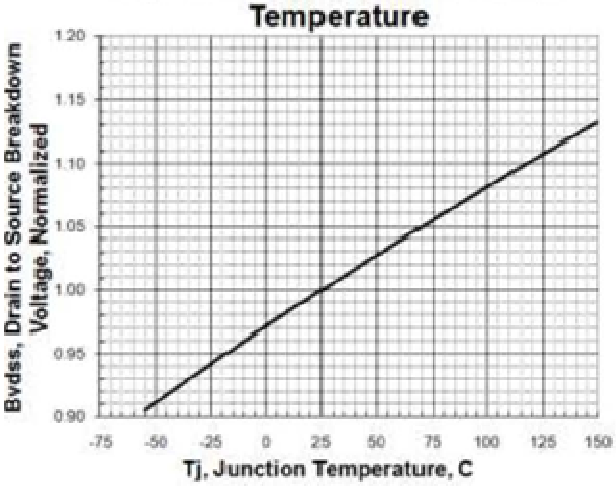


Figure 12.Threshold Voltage vs Temperature

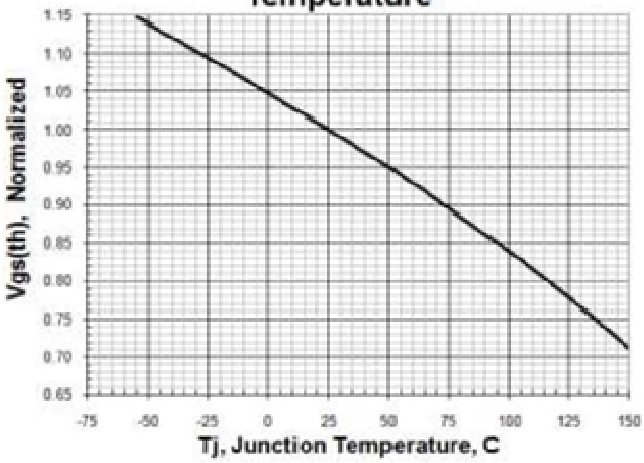


Figure 13 . Maximum Safe Operating Area

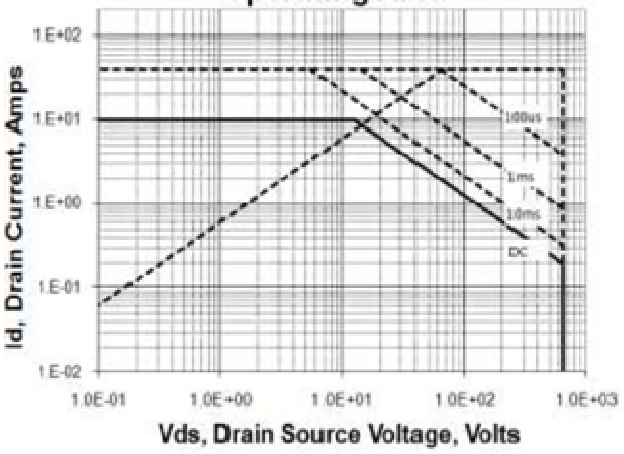


Figure 14. Capacitance vs Vds

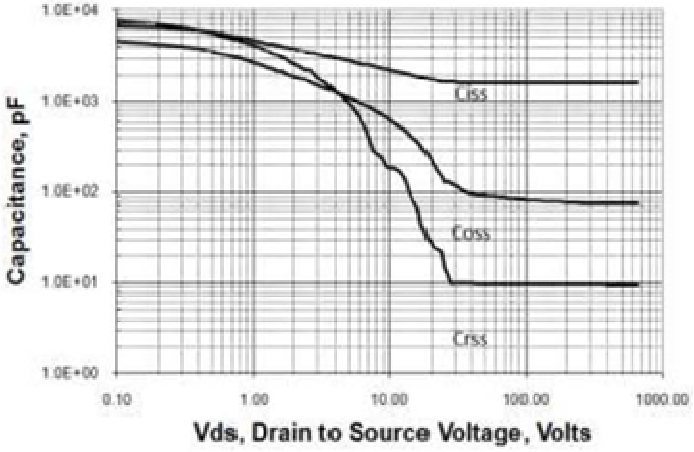


Figure 15 .Typical Gate Charge

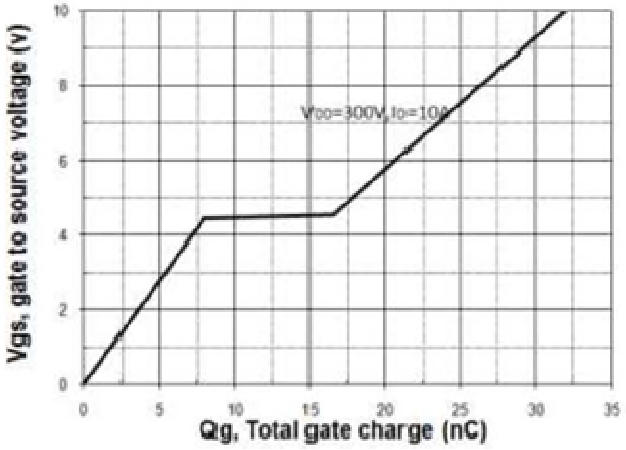
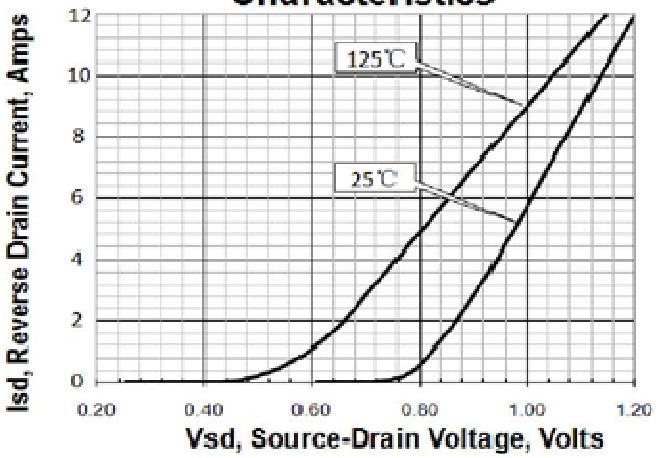


Figure 16.Body Diode Transfer Characteristics



9. Test Circuits and Waveforms

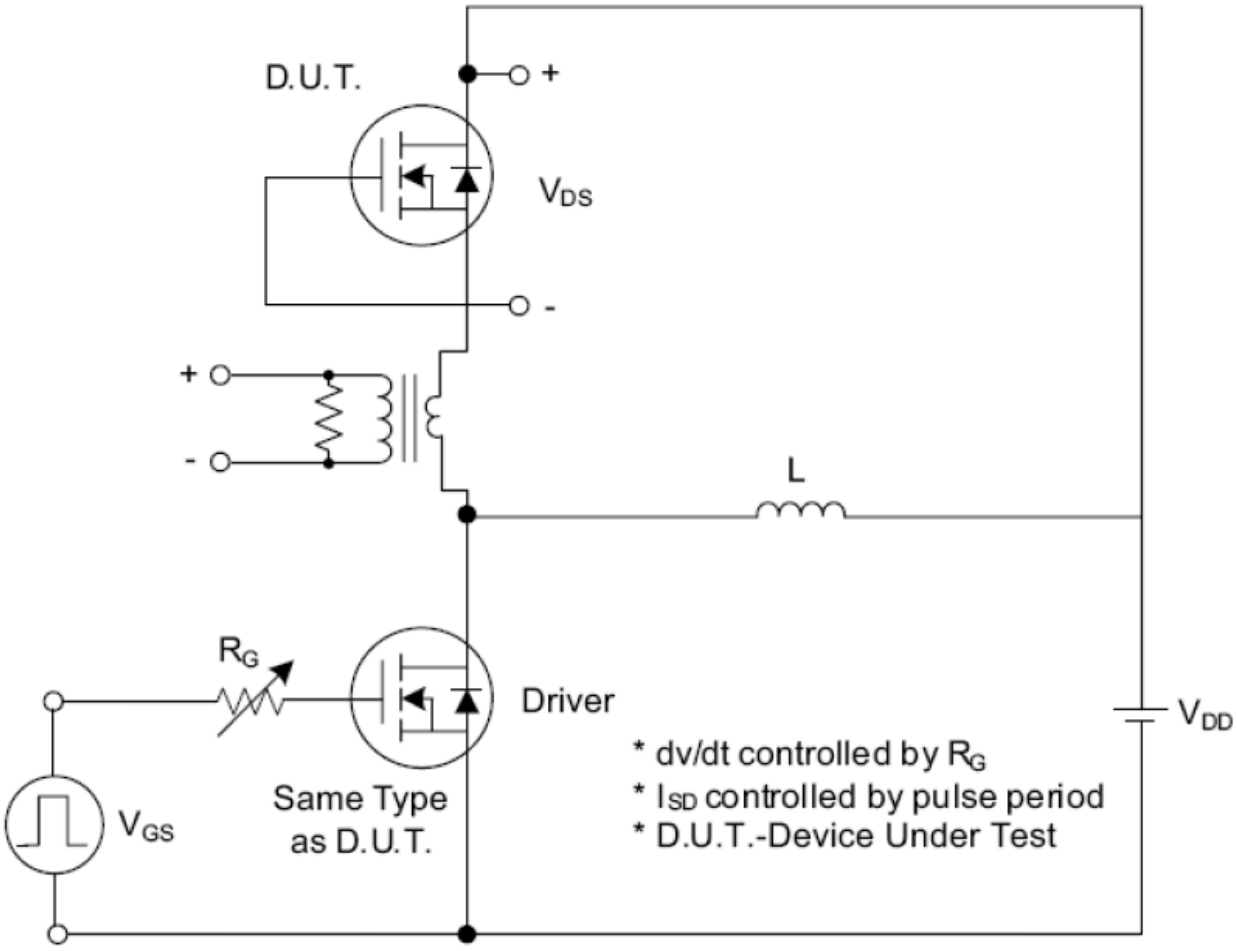


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

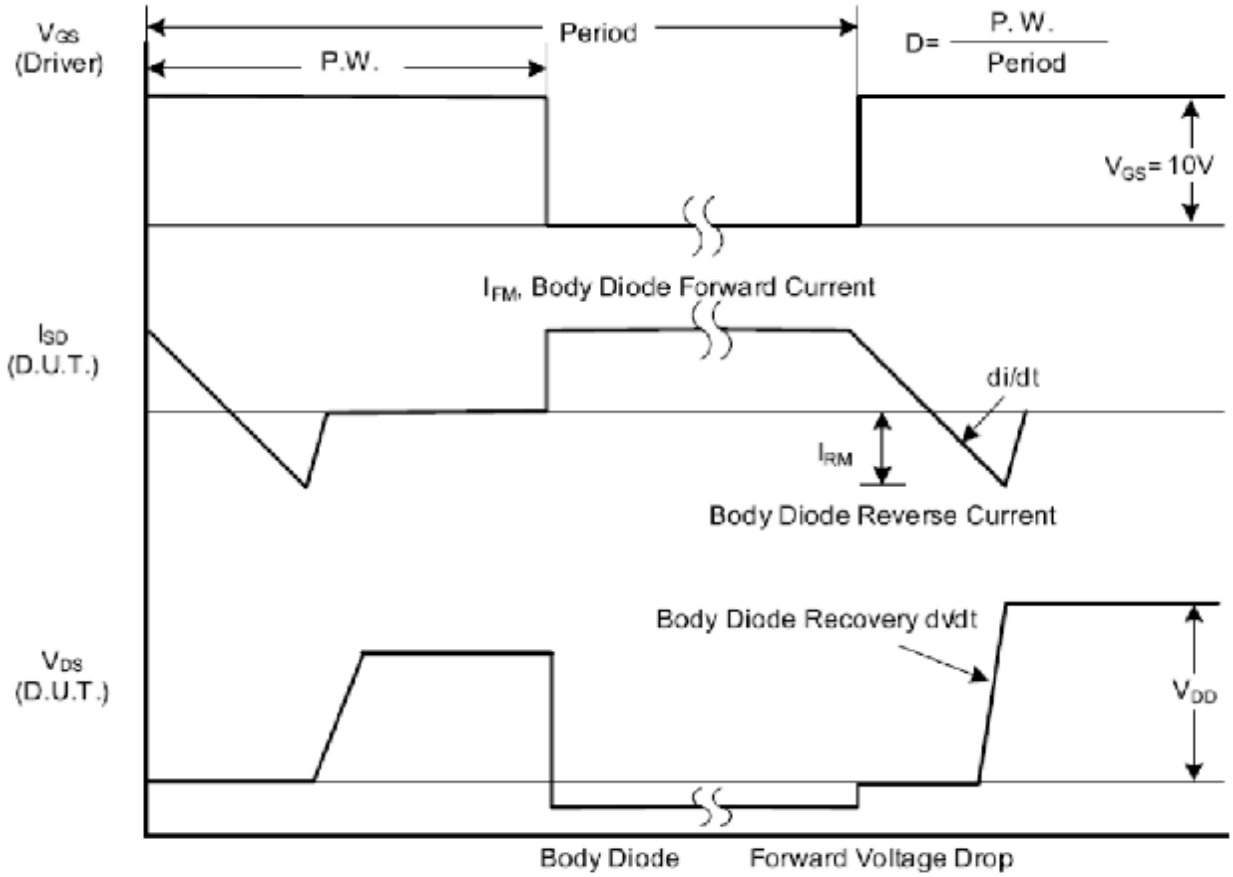


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

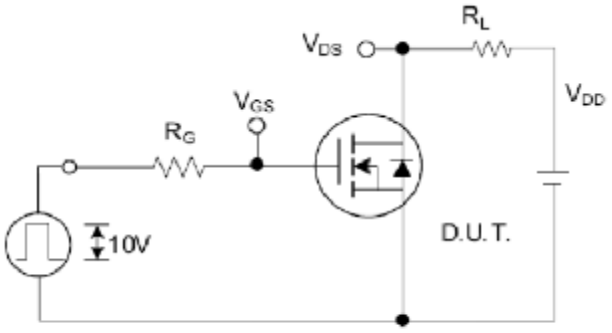


Fig. 2.1 Switching Test Circuit

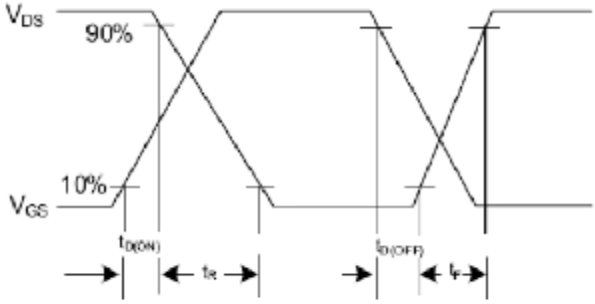


Fig. 2.2 Switching Waveforms

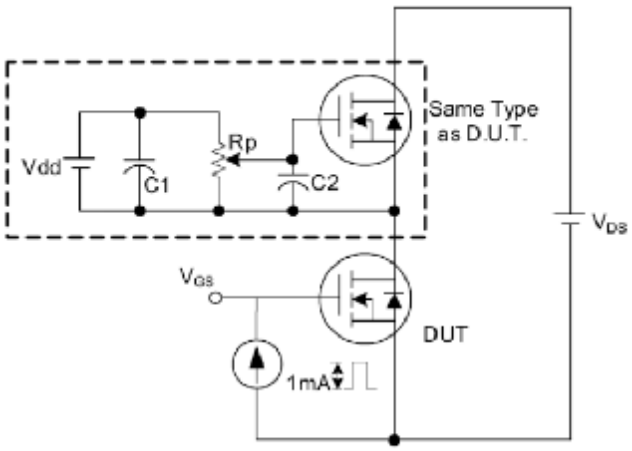


Fig. 3 . 1 Gate Charge Test Circuit

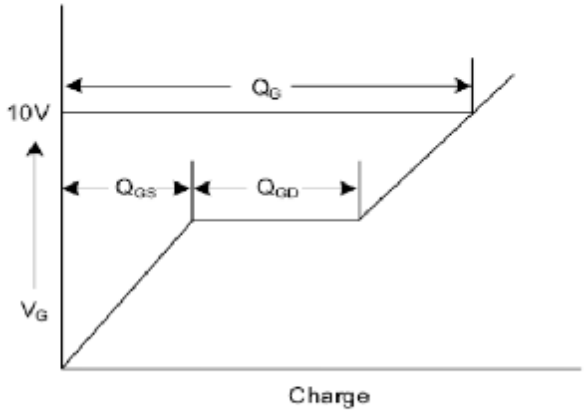


Fig. 3 . 2 Gate Charge Waveform

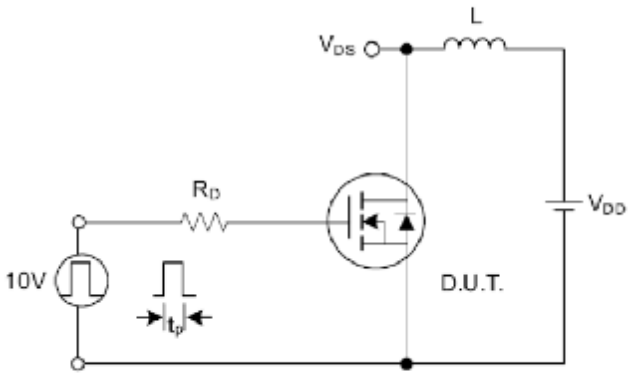


Fig. 4.1 Unclamped Inductive Switching Test Circuit

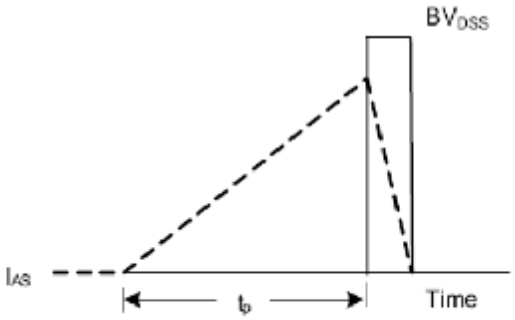


Fig. 4.2 Unclamped Inductive Switching Waveforms